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(71) Applicant:
SHINKO ELECTRIC INDUSTRIES CO. LTD.
Nagano-shi, Nagano 380-0921 (JP)

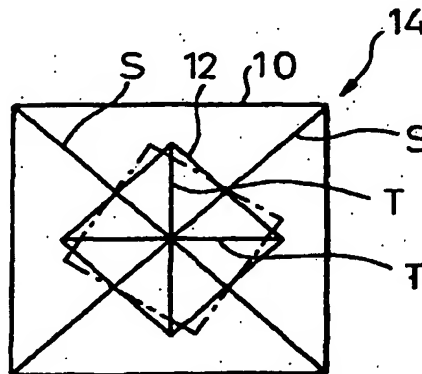
(72) Inventor:
MURAYAMA, Kei,
Shinko Electric Industr. Co., Ltd.
Nagano 380-0921 (JP)

(74) Representative:
Rackham, Stephen Neil
GILL JENNINGS & EVERY,
Broadgate House,
7 Eldon Street
London EC2M 7LH (GB)

(54) SEMICONDUCTOR DEVICE

(57) A semiconductor device 14 capable of reducing the warpage in a substrate is provided. A semiconductor chip 12 is mounted on a substrate 10 made of an electro-insulating material by flip-chip bonding, so that connector terminals formed on the substrate 10 are connected to electrodes of the semiconductor chip 12 and a gap between the substrate 10 and the semiconductor chip 12 is filled with an underfiller 18. According to the present invention, in the semiconductor device 14, none of sides of the substrate 10 is parallel to any one of sides of the semiconductor chip 12, and none of diagonal lines S of the substrate 10 coincides with any one of diagonal lines T of the semiconductor chip 12.

Fig. 3



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Description

TECHNICAL FIELD

[0001] The present invention relates to a semiconductor device wherein a semiconductor chip is mounted onto a substrate by flip-chip bonding and is fixed thereto via an adhesive means.

BACKGROUND ART

[0002] A general structure of a semiconductor device 14 wherein a semiconductor chip 12 is mounted on a substrate 10 made of an electro-insulating material will be described with reference to Fig. 1 and Fig. 2(c) which is a sectional view taken along line A-A in Fig. 1.

[0003] In this regard, flip-chip bonding is a method for bonding the semiconductor chip 12 onto the substrate 10 while a surface of the former carrying active elements thereon is opposed to the substrate 10. In general, solder bumps 16 are formed as electrodes on the semiconductor chip 12 which is reversed upside down and positioned in place on the substrate 10, after which the solder bumps 16 are molten all together to connect the electrodes with connector terminals (not shown) formed on the substrate 10 and secure the semiconductor chip 12 on the substrate 10. Since the solder bumps are arranged not only on the periphery of the semiconductor chip 12 but also at any positions thereon, it is possible to easily obtain as many input/output terminals (I/O) as needed.

[0004] Also, since the semiconductor chip 12 is directly mounted on the substrate 10 via solder, there may be cases wherein an underfiller 18 (such as epoxy type resin) is filled in a gap between the substrate 10 and the surface of the semiconductor chip 12 carrying the active elements thereon to reinforce the bonding for the purpose of improving the reliability (strength) of the connecting portion.

[0005] When the flip-chip bonding is carried out, an anisotropic electro-conductive film or anisotropic electro-conductive adhesive having the same adhesive property as the underfiller may be used instead of the latter for bonding the semiconductor chip 12 to the substrate 10. Specifically, a semiconductor chip provided with Au stud bumps prepared by the Au wire-bonding and the substrate coated with the anisotropic electro-conductive adhesive or clad with the anisotropic electro-conductive film is prepared. The semiconductor chip is placed on the substrate via the anisotropic electro-conductive adhesive or the anisotropic electro-conductive film, and the assembly is heated under pressure to connect the semiconductor chip with the substrate. In this regard, the anisotropic electro-conductive adhesive or film contains nickel particles having a size of 3 μm order in epoxy type resin and is cured by heat in the same manner as in the underfiller.

[0006] The above-mentioned prior art semiconductor

device 14, however, has the following problems.

[0007] The substrate 10 or the semiconductor chip 12 is preferably of a square shape. This is because when a so-called constant-size substrate of a rectangular shape (including a square shape) is cut into individual square substrates 10, or when a sliced silicon wafer of a predetermined diameter is cut into individual square semiconductor chips 12, as many substrates 10 or semiconductor chips 12 as possible are obtainable with least waste, and also the square shape facilitates the patterning efficiency of circuit patterns formed thereon.

[0008] The semiconductor chip 12 is mounted onto the substrate 10 so that each of sides of the semiconductor chip 12 is parallel to the corresponding side of the substrate 10. In addition, generally, the semiconductor chip 12 is mounted onto the substrate 10 so that a center of the former coincides with that of the latter. See Fig. 1.

[0009] When the semiconductor device 14 is mounted onto an originally flat circuit board (not shown), the semiconductor device 14 itself is preferably of a flat shape to enhance the reliable connection between the circuit board and the substrate 10.

[0010] As described before, the connecting portion between the substrate 10 and the semiconductor chip 12 is reinforced, for the purpose of improving the durability or reliability thereof, by the underfiller 18 or the anisotropic electro-conductive adhesive or film which is formed of thermosetting resin and cured through a curing process. Actually, the substrate 10 often warps after the curing process.

[0011] This warpage phenomenon of the substrate 10 will be explained with reference to Figs. 2(a) to 2(c) illustrating states prior to, during and after the curing process, respectively. While the explanation is made on a case wherein the underfiller is used as adhesive interposed between the semiconductor chip 12 and the substrate 10, the same is true to other cases wherein the anisotropic electro-conductive adhesive or film is used instead thereof.

[0012] First, in a state shown in Fig. 2(a) wherein the semiconductor chip 12 is merely placed on the substrate 10 prior to the curing process, no substantial warpage occurs both in the substrate 10 and the semiconductor chip 12. That is, an amount of warpage is approximately equal to that in the substrate 10 when it stands alone.

[0013] Next, during the curing process wherein the underfiller 18 filled in the gap between the substrate 10 and the semiconductor chip 12 is cured, the substrate 10 thermally extends at a high temperature. However, since the underfiller 18 is completely cured after the substrate 10 has fully expanded, no substantial warpage occurs also in both thereof even in this curing process. See Fig. 2(b).

[0014] Finally, in a passage wherein a temperature of the assembly is lowering to a normal temperature, the fully extended substrate 10 gradually contracts as the

temperature lowers. Since an amount of contraction of a region B of the substrate 10 in which the semiconductor chip 12 is placed (bonded) (in other words, a region of the substrate 10 in contact with the underfiller 18) is smaller than an amount of contraction of the remaining region of the substrate 10 because the thermal expansion coefficient of the semiconductor chip 12 is smaller than that of the substrate 10. Accordingly, when viewed from a lateral side, a surface of the substrate 10 (a back surface) opposite to a surface thereof including the region B carrying the semiconductor chip 12 therein (a front surface) more contracts than the front surface, whereby the substrate 10 warps so that the back surface thereof is concave as shown in Fig. 2(c).

[0015] This warpage of the substrate 10; i.e., the warpage of the semiconductor device 14; has the following relationship with the region B carrying the semiconductor chip 12.

[0016] First, the warpage of the substrate 10 is a phenomenon caused by a fact wherein the region B of the substrate 10 in contact with the underfiller 18 could not fully contract to an extent corresponding to the original thermal expansion coefficient thereof, and therefore, the warpage occurs with the region B as a center; specifically, it occurs in the radial direction all over the substrate 10 from the central point of the region B. Assuming the warpage of the substrate 10 along an imaginary straight line L passing by the central point of the region B, there is a relationship in that the longer a segment of the straight line L in the region B, the more the warpage.

[0017] Second, assuming again that the warpage of the substrate 10 is along the imaginary line L, since the substrate 10 warps to be a generally U-shape as a whole with the region B as a center as mentioned above, the maximum displacement in the substrate 10 due to the warpage occurs at the intersection of the imaginary straight line L and a contour of the substrate 10 farthest from the region B. In the square-shaped substrate 10, the above-mentioned intersection farthest from the region B is resulted when the imaginary straight line L coincides with a diagonal line of the substrate 10; in other words, such an intersection exists at the respective corner of the substrate 10. That is, the maximum warpage generates between a pair of corners of the substrate 10 located opposite to each other along a diagonal line.

[0018] In the prior art semiconductor device 14, both of the substrate 10 and the semiconductor chip 12 are of a square shape, and the semiconductor chip 12 is mounted to the substrate 10 with the respective sides of the substrate 10 being parallel to those of the semiconductor chip 12 and with the center of the substrate coinciding with that of the semiconductor chip 12. Since the diagonal line of the substrate 10 coincides with that of the semiconductor chip 12, a length of the region B on the diagonal line, along which the warpage of the substrate 10 is maximum, is longest. Thus, it is likely that

the generation of large warpage occurs at four corners of the substrate 10.

DISCLOSURE OF THE INVENTION

[0019] The present invention has been made to solve the above-mentioned problems in the prior art, and an object of the present invention is to provide a semiconductor device capable of reducing the warpage of a substrate.

[0020] To achieve such an object, according to the present invention, a semiconductor device, comprising a substrate made of an electro-insulating material and having connector terminals on the surface thereof, a semiconductor chip to be mounted to the substrate and having electrodes to be flip-chip bonded with the connector terminals, and adhesive means filled in a gap between the substrate and the semiconductor chip is provided, characterized in that

none of sides of the substrate as seen in a plan view is parallel to any one of sides of the semiconductor chip as seen in a plan view, and none of diagonal lines of the substrate as seen in a plan view coincides with any one of diagonal lines of the semiconductor chip as seen in a plan view.

[0021] According to this semiconductor device, a length of a region of the substrate in contact with the adhesive means measured along the diagonal line on which the maximum warpage would occur in the substrate is apparently smaller in comparison with a prior art semiconductor device wherein the diagonal lines of the substrate and the semiconductor chip just coincide with each other. Thereby, it is possible to reduce the warpage at the opposite ends of the diagonal line of the substrate; i.e., at the corners thereof. More concretely, while most of the semiconductor chip and the substrate are of a square shape or a rectangular shape, even in such a case, it is possible to reduce the warpage of the substrate at the corner thereof by such an arrangement that none of the respective sides of the substrate is parallel to any one of the sides of the semiconductor chip, and none of the respective diagonal lines of the substrate coincides with any one of the diagonal lines of the semiconductor chip.

[0022] Also, if the semiconductor chip is mounted onto the substrate so that either one of sides of the semiconductor chip is parallel to either one of diagonal lines of the substrate, a length of a region of the substrate carrying the semiconductor chip measured along a diagonal line of the substrate becomes a minimum, whereby the amount of warpage is least.

[0023] As the adhesive means, either of underfiller, anisotropic electro-conductive adhesive or anisotropic electro-conductive film having an adhesivity, each comprised of epoxy type resin, may be used. It is possible to obtain an equivalent effect for reducing the warpage by

using any of the adhesive means described above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024]

Fig. 1 is a plan view illustrating a contour of one example of a prior art semiconductor device; Figs. 2(a), 2(b) and 2(c) are sectional views taken along a line A-A in Fig. 1, illustrating a sequence of a process for producing the prior art semiconductor device, respectively; Fig. 2(a) showing a state wherein a semiconductor chip is mounted onto a substrate by a flip-chip bonding, Fig. 2(b) showing a state wherein an underfiller is filled in a gap, and Fig. 2(c) showing a state wherein the underfiller is cured and then cooled to a normal temperature; Fig. 3 is a plan view of a first embodiment of a semiconductor device according to the present invention;

Figs. 4(a) and 4(b) are plan views of a second embodiment of a semiconductor device according to the present invention illustrating the relationship between a substrate and a region, respectively; Fig. 4(a) showing a state wherein the semiconductor chip is mounted onto the substrate so that sides of the both are parallel to each other, and Fig. 4(b) showing a state wherein the semiconductor chip is inclined relative to the substrate;

Figs. 5(a), 5(b) and 5(c) are plan views of a third embodiment of a semiconductor device according to the present invention illustrating the relationship between a substrate and a region, respectively; Fig. 5(a) showing a state wherein the semiconductor chip is mounted onto the substrate so that sides of the both are parallel to each other, Fig. 5(b) showing a state wherein the semiconductor chip is made to rotate so that one of diagonal lines of the semiconductor chip coincides with one of diagonal lines of the substrate, and Fig. 5(c) showing a state wherein the semiconductor chip is made to further rotate to incline the semiconductor chip relative to the substrate so that none of the diagonal lines coincide with each other;

Fig. 6 is an illustration for explaining a concept of corners of a substrate or a semiconductor chip;

Figs. 7(a) to 7(d) are sectional views, respectively, illustrating various types of a complete semiconductor device according to the present invention;

Fig. 8 is a sectional view of a semiconductor device according to the present invention mounted to a mother board; and

Figs. 9(a) and 9(b) are a table and graphs, respectively, showing comparison data of warpage between the semiconductor device of the first embodiment and the prior art semiconductor device.

BEST MODES FOR CARRYING OUT THE INVENTION

[0025] The preferred embodiments of a semiconductor device according to the present invention will be described in detail below with reference to the attached drawings.

[0026] While an underfiller is used as adhesive interposed between a substrate 10 and a semiconductor chip 12 in the following embodiments, an anisotropic electro-conductive adhesive or anisotropic electro-conductive film may be used as described with reference to the prior art.

(First Embodiment)

[0027] A structure of a semiconductor device 14 will be described with reference to Fig. 3.

[0028] Contours of a substrate 10 and a semiconductor chip 12 constituting the semiconductor device 14 are of a square shape. The semiconductor chip 12 is mounted onto the substrate 10 by flip-chip bonding so that a center of the semiconductor chip 12 coincides with that of the substrate 10, and fixedly adhered by an underfiller 18.

[0029] In the prior art semiconductor device 14, as shown in Fig. 1, the respective sides of the substrate 10 and the semiconductor chip 12 are parallel to each other and the respective diagonal lines T of the semiconductor chip 12 coincide with two diagonal lines S of the substrate 10 (i.e., corners of the semiconductor chip 12 are positioned on the diagonal lines S of the substrate 10). On the contrary, according to this embodiment, as shown in Fig. 3, the semiconductor chip 12 is inclined relative to the substrate 10 so that a diagonal line T of the semiconductor chip 12 is deviated from a diagonal line S of the substrate 10. As an example, in this embodiment, the inclination angle is 45 degrees. In this state, none of the corners of the semiconductor chip 12 is positioned on the diagonal line S of the substrate 10, and a length of a region B (contact region) of the substrate 10 in contact with the underfiller 1 measured along the diagonal line S becomes minimum, because the diagonal line S is parallel or orthogonal to the respective sides of the semiconductor chip 12. Accordingly, the warpage of the substrate 10 along the diagonal line S becomes least. That is, an overall warpage of the semiconductor device 14 also becomes least.

[0030] In this regard, the semiconductor chip 12 is inclined at 45 degrees in this embodiment so that the warpage of the substrate 10 along the diagonal line S becomes least. Different inclination angles, however, may be selected as shown in Fig. 3 by a chain line unless the diagonal line T of the semiconductor chip 12 coincides with the diagonal line S of the substrate 10. Even in the latter case, the warpage of the semiconductor device 14 is always less than that in the prior art semiconductor device.

(Second Embodiment)

[0031] A structure of this semiconductor device 14 will be described with reference to Fig. 4.

[0032] Contours of a substrate 10 and a semiconductor chip 12 constituting the semiconductor device 14 are of a rectangular shape and similar to each other. The semiconductor chip 12 is mounted onto the substrate 10 by a flip-chip bonding so that a center of the semiconductor chip 12 coincides with that of the substrate 10, and is fixedly adhered by an underfiller 18.

[0033] Similar to the first embodiment, the prior art semiconductor device 14 shown in Fig. 4(a) wherein each side of the substrate 10 is parallel to each side of the semiconductor chip 12 is modified so that the respective diagonal lines T of the semiconductor chip 12 do not coincide with the respective diagonal lines S of the substrate 10 by inclining the semiconductor chip 12 relative to the substrate 10 as shown in Fig. 4(b). Thereby, a length of a contact region B of the substrate 10 in contact with the underfiller 18 measured along the diagonal line S, which causes the warpage, becomes shorter in comparison with the prior art semiconductor device 14, and therefore the warpage of the substrate 10 along the diagonal line S becomes least. Accordingly, an overall warpage of the substrate 10 as well as the semiconductor device 14 is also reduced.

[0034] In this embodiment, to reduce the warpage of the substrate 10 to a maximum extent, the semiconductor chip 12 is made to incline relative to the substrate 10 so that one of sides of the semiconductor chip 12, particularly a longer side in this case, is parallel to the diagonal line S, as shown in Fig. 4(b) by a chain line. In such a state, a length of the contact region B measured along the diagonal line S of the substrate 10 becomes shortest. Regarding the first embodiment, since the semiconductor chip 12 is of a square shape, there is no distinction between a shorter side and a longer side. Even in this case, supposing that one pair of opposite sides constitute longer sides; it could also be said that a length of the contact region B measured along the diagonal line S of the substrate 10 becomes shortest if the longer side is parallel to the diagonal line S, resulting in the least warpage.

(Third Embodiment)

[0035] A structure of this semiconductor device 14 will be described with reference to Fig. 5.

[0036] Contours of a substrate 10 and a semiconductor chip 12 constituting the semiconductor device 14 are not similar; i.e., the semiconductor chip 12 is of a square shape and the substrate 10 is of a rectangular shape, for example. The semiconductor chip 12 is mounted onto the substrate 10 by a flip-chip bonding so that a center of the semiconductor chip 12 coincides with that of the substrate 10 and is fixedly adhered by an underfiller 18.

[0037] According to this embodiment, even in the prior art semiconductor device 14 shown in Fig. 5(a) wherein each side of the substrate 10 is parallel to each side of the semiconductor chip 12, the respective diagonal lines T of the semiconductor chip 12 do not coincide with the respective diagonal lines S of the substrate 10. Therefore, the warpage of the substrate 10 along the diagonal line T becomes less in comparison with a case shown in Fig. 5(b) wherein the semiconductor chip 12 is made to incline relative to the substrate 10 so that one of the diagonal lines T of the semiconductor chip 12 coincides with one of the diagonal lines S of the substrate 10.

[0038] If the semiconductor chip 12 is made to further incline in the same direction from the state shown in Fig. 5(b) so that a pair of longer sides of the semiconductor chip 12 (i.e., one of two pairs of opposite sides since the semiconductor chip 12 is of a square shape in this embodiment) are parallel to one of diagonal lines S of the substrate 10, a length of a region B of the substrate 10 in contact with the underfiller 18 measured along this diagonal line S, which causes the warpage, becomes shortest, resulting in the least warpage generated along the diagonal line S of the substrate 10.

[0039] There is a contour of a semiconductor chip 12 or a substrate 10 as shown in Fig. 6 wherein corners thereof are cut off. In such a semiconductor chip 12 or substrate 10, an imaginary corner D is conveniently defined by an intersection between extensions of the respective sides, and a diagonal line is defined by a straight line connecting these imaginary corners D with each other.

[0040] Although not specifically described, when the semiconductor chip 12 is inclined relative to the substrate 10, positions of a group of connector pads formed on the substrate 10 must, of course, be inclined as a whole in correspondence thereto.

[0041] Figs. 7(a) to 7(d) illustrate various types of a completed semiconductor device according to the present invention, particularly classified in accordance with kinds of substrates. Fig. 7(a) is a semiconductor device of a ball grid array type wherein solder bumps 30 are used also in the substrate 10 as external connector terminals. Fig. 7(b) is a semiconductor device of a pin grid array type wherein pins 20 are used in the substrate 10 as external connector terminals. Fig. 7(c) is a semiconductor device of a land grid array type wherein lands 22 are used as external connector terminals. Fig. 7(d) is a semiconductor device of a ball grid array type wherein Au stud bumps are used as electrodes 24 of the semiconductor chip 12, and an anisotropic electro-conductive film 26 is used as adhesive means.

[0042] Fig. 8 illustrates a semiconductor device according to the present invention mounted onto a mother board 28. While this semiconductor device is of a ball grid array type shown in Fig. 7(a), other types may be mounted onto the mother board 28 in the same manner. In this case, since the warpage of the substrate 10

is reduced as described above, a stress in the connection between the solder bumps 30 of the substrate 10 and the mother board 28 becomes smaller.

[0043] Next, as shown in Figs. 9(a) and 9(b), five samples of the prior art semiconductor device (Nos. 3, 2, 8, 6 and 4) and five samples of the semiconductor device according to the first embodiment (Nos. 5, 9, 1, 7 and 10) were prepared for the purpose of comparison. They were tested to determine the warpage in an initial state wherein the semiconductor chip 12 is merely mounted onto the substrate 10 and the warpage in a final state after the underfiller 18 has been filled and cured, from which is obtained the respective difference in warpage (DELTA) from the initial state to the final state. A size of the semiconductor chip 12 was 15 mm x 15 mm, and that of the substrate 10 was 40 mm x 40 mm. The warpage was measured by a non-contact type tester (RVSI; LS-3900DB).

[0044] Upon the selection of the respective samples, care was taken so that the samples of the prior art semiconductor device (shown in Fig. 1) and those of the semiconductor device according to the present invention (shown in Fig. 3) respectively include one having, in the initial state, the same tendency in the direction and amount of the warpage.

[0045] As apparent from the test results, the semiconductor device according to the present invention is always less in DELTA than the prior art semiconductor device between the respective pair of samples of the same tendency (5 and 3; 9 and 2; 1 and 8; 7 and 6; and 10 and 4), which exhibits the favorable effect of the present invention. In a table of Fig. 9(a), curves in a column of DIRECTION, Initial State and Final State illustrate profiles of warpage, as seen in the lateral direction, in the initial and final states of the semiconductor device carrying the semiconductor chip on the upper side.

[0046] While the present invention was described above with reference to the preferred embodiments, it should be noted that the present invention is not limited to the above-mentioned embodiments but includes various changes and modifications without departing from a spirit of the invention.

CAPABILITY OF EXPLOITATION IN INDUSTRY

[0047] According to the semiconductor device of the present invention, a length of the contact region of the substrate in contact with the adhesive measured along a diagonal line of the substrate, which is likely to cause the maximum warpage, becomes always shorter in comparison with the prior art semiconductor device wherein diagonal lines of the substrate and the semiconductor chip coincide with each other. Accordingly, it is possible to reduce the warpage at opposite ends of the diagonal line of the substrate; i.e., the corners thereof; resulting in the reduction in an overall warpage of the semiconductor device.

[0048] In addition, the warpage becomes even less if

the semiconductor chip is mounted onto the substrate so that one of sides thereof is parallel to one of diagonal lines of the substrate, because a length of the region of the substrate for mounting the semiconductor chip measured along the diagonal line of the substrate becomes a minimum.

[0049] The present invention is in particular suitably applicable to a semiconductor device of a ball grid array type and a land grip array type which is particularly required to have a flatness when mounted to a mother board 28, because if the substrate 10 is warped, there are solder bumps or lands incapable of being connected to the mother board 28.

EXPLANATION OF REFERENCE NUMERALS

[0050]

10	substrate
12	semiconductor chip
14	semiconductor device
16	solder bump
18	underfiller
20	pin
22	land
24	Au stud bump
26	anisotropic electro-conductive film
28	mother board
S	diagonal line of substrate
T	diagonal line of semiconductor chip

Claims

1. A semiconductor device comprising a substrate made of an electro-insulating material and having connector terminals on a surface thereof, a semiconductor chip mounted on the substrate and having electrodes to be flip-chip bonded with the connector terminals, and adhesive means filled in a gap between the substrate and the semiconductor chip, characterized in that

none of sides of the substrate as seen in a plan view is parallel to any one of sides of the semiconductor chip as seen in a plan view, and none of diagonal lines of the substrate as seen in a plan view coincides with any one of diagonal lines of the semiconductor chip as seen in a plan view.

2. A semiconductor device as defined by claim 1, characterized in that both contours of the semiconductor chip and of the substrate are of a square shape or a rectangular shape.
3. A semiconductor device as defined by claim 1, characterized in that either one of the sides of the semiconductor chip is parallel to either one of the

diagonal lines of the substrate.

4. A semiconductor device as defined by claim 1, characterized in that the adhesive means is an underfiller comprised of epoxy type resin.
5. A semiconductor device as defined by claim 1, characterized in that the adhesive means is an anisotropic electro-conductive adhesive.
6. A semiconductor device as defined by claim 1, characterized in that the adhesive means is an anisotropic electro-conductive film having an adhesivity.

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Fig. 1

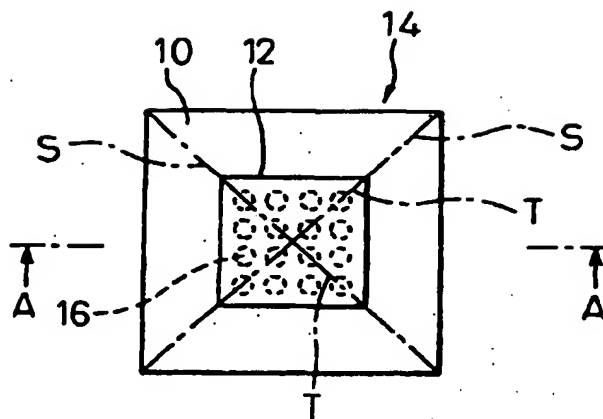


Fig.2(a)

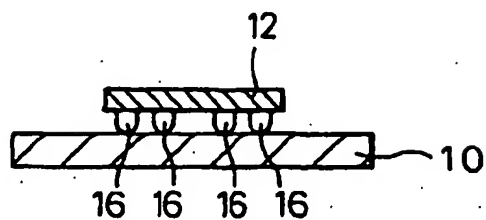


Fig.2(b)

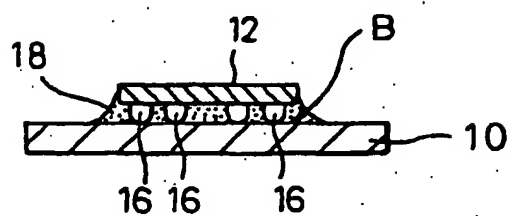


Fig.2(c)

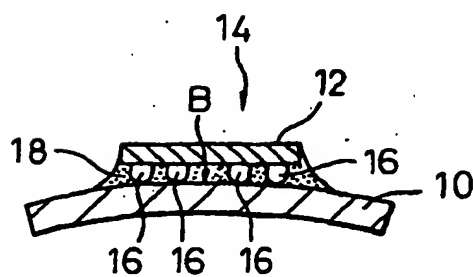


Fig. 3

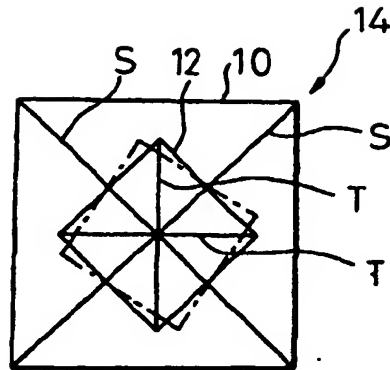


Fig. 4(a)

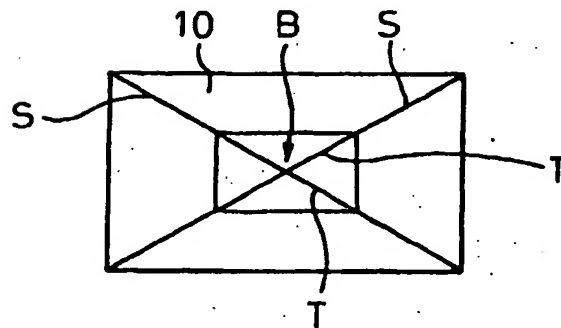


Fig. 4(b)

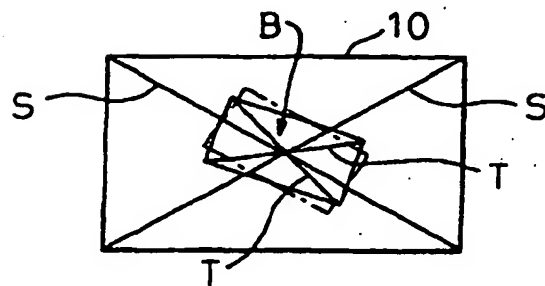


Fig.5(a)

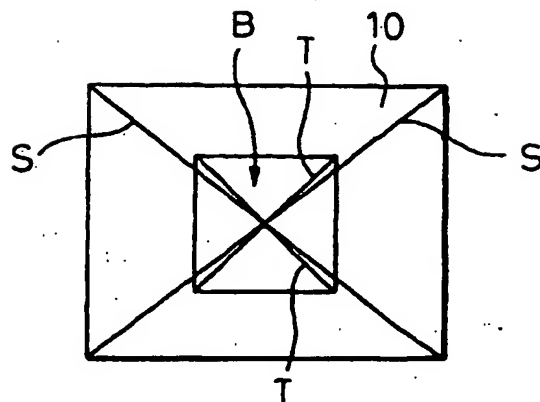


Fig.5(b)

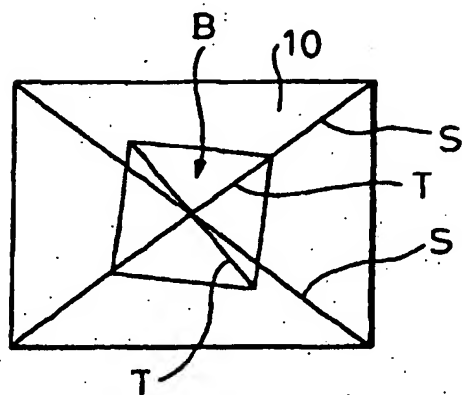


Fig.5(c)

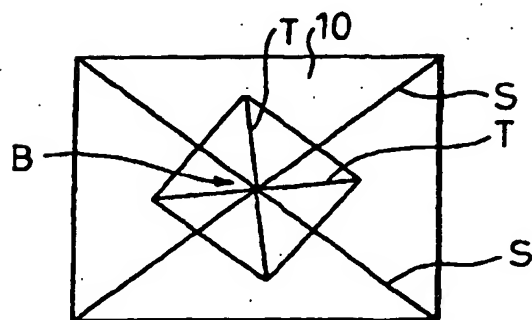


Fig.6

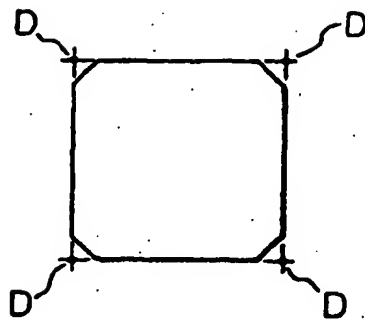


Fig. 7(a)

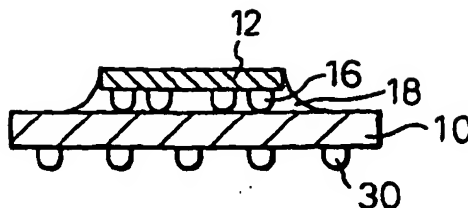


Fig. 7(b)

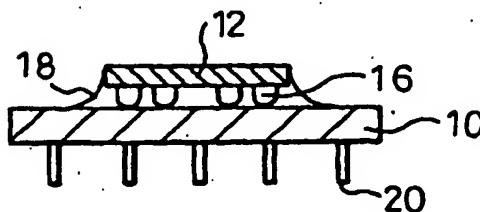


Fig. 7(c)

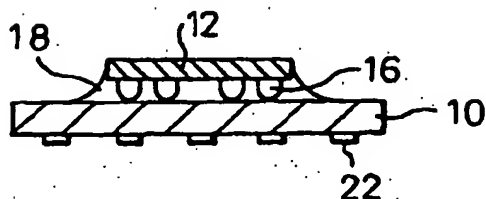


Fig. 7(d)

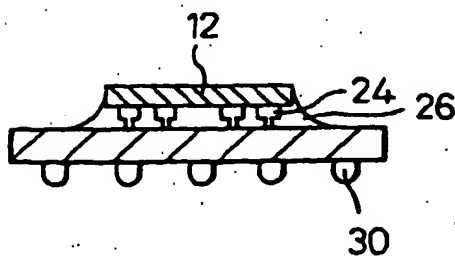


Fig. 8

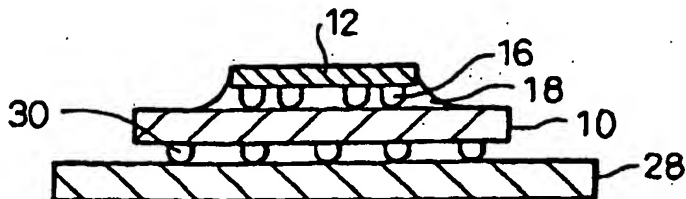


Fig. 9(a)

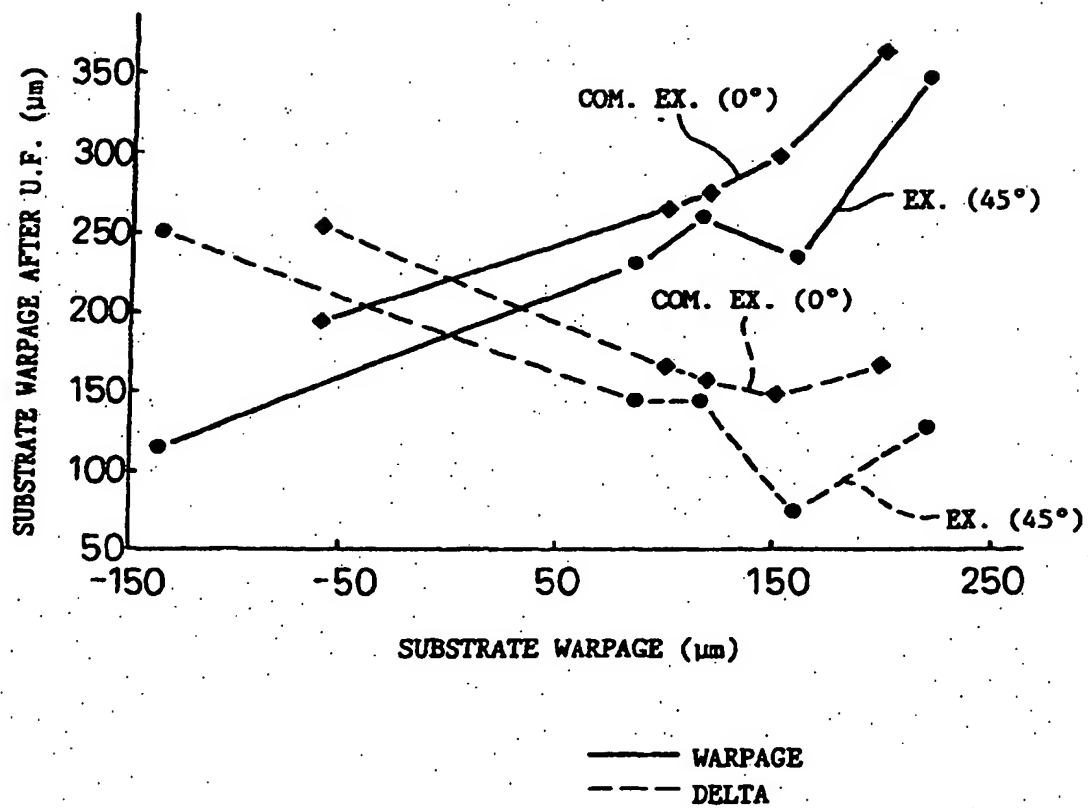
COMPARISON BETWEEN CHIP MOUNTING POSITIONS

INCLINATION ANGLE (°)	SAMPLE NO.	FLATNESS		DIRECTION	
		INITIAL STATE	FINAL STATE	DELTA	INITIAL STATE FINAL STATE
0	5	-61.1	194.6	255.7	()
	9	100.7	267.0	166.3	()
	1	119.1	276.1	157.0	()
	7	151.6	299.4	147.8	()
	10	199.0	365.8	166.8	()
45	3	-135.9	115.0	250.9	()
	2	86.6	230.8	144.2	()
	8	116.2	260.2	144.0	()
	6	159.8	234.8	75.0	()
	4	220.0	347.7	127.7	()

COMPARATIVE
EXAMPLES

EXAMPLES

Fig.9(b)



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP98/05888

A. CLASSIFICATION OF SUBJECT MATTER Int.Cl. ⁶ H01L21/60		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) Int.Cl. ⁶ H01L21/60		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Jitsuyo Shinan Koho 1926-1996 Toroku Jitsuyo Shinan Koho 1994-1999 Kokai Jitsuyo Shinan Koho 1971-1999 Jitsuyo Shinan Toroku Koho 1996-1999		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP, 4-28243, A (Mitsubishi Electric Corp.),	1-3
Y	30 January, 1992 (30. 01. 92), Claims ; Fig. 2 (Family: none)	4-6
Y	JP, 8-236578, A (NEC Corp.), 13 September, 1996 (13. 09. 96), Fig. 4 (Family: none)	4
Y	JP, 4-292803, A (Hitachi, Ltd.), 16 October, 1992 (16. 10. 92), Fig. 1 (Family: none)	5, 6
A	JP, 3-171645, A (Hitachi Cable, Ltd.), 25 July, 1991 (25. 07. 91) (Family: none)	1-6
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
A Special categories of cited documents: document defining the general state of the art which is not considered to be of particular relevance *B* earlier document but published on or after the international filing date document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reasons (as specified) *O* document referring to an oral disclosure, use, exhibition or other means *P* document published prior to the international filing date but later than the priority date claimed *T* later documents published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art *Z* document member of the same patent family		
Date of the actual completion of the international search 24 March, 1999 (24. 03. 99)		Date of mailing of the international search report 6 April, 1999 (06. 04. 99)
Name and mailing address of the ISA/ Japanese Patent Office		Authorized officer
Facsimile No.		Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)